50.   (Previously Presented) The method of Claim 49 comprising shifting predecoded lines coupled to at least one of said first and second predecoders.

51.   (Previously Presented) The method of Claim 49 comprising using shifting circuitry coupled to at least one of said first and second predecoders.

52.   (Previously Presented) The method of Claim 49 comprising at least one higher address predecoded line coupled to at least one of said first and second predecoders.

53.   (Previously Presented) The method of Claim 53 comprising at least one lower address predecoded line coupled to at least one of said first and second predecoders and paired with said at least one higher address predecoded line.

54.   (Previously Presented) The method of Claim 49 comprising at least one of said first predecoders adapted to fire for current address mapping.

55.   (Previously Presented) The method of Claim 49 comprising said at least one second predecoder adapted to fire for previous address mapping.

56.   (Previously Presented) The method of Claim 49 comprising shifting in said second predecoder using shift circuitry.

57.   (New) A method of providing redundancy in a hierarchical memory structure, comprising:

        identifying at least one predecoder as a predecoder for shifting out; and

        shifting out said identified at least one predecoder.

58.   (New) The method of Claim 57 comprising shifting in at least one other predecoder.

59.   (New) The method of Claim 58 comprising shifting predecoded lines coupled to at least one of said at least one predecoder and said at least one other predecoder.

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